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Gururaj Nagendra

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EXAMINER

FATEHI, PARHAM R

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2194

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/783,840	<b>Applicant(s)</b> NAGENDRA ET AL.	
	<b>Examiner</b> PAUL R. FATEHI	<b>Art Unit</b> 2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11/30/2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1-27 are pending in this application. This Office Action is responsive to communication filed 11/30/2007.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-10, 12-18 and 21-22 are rejected under 35 U.S.C. 102(e) as being disclosed by Brumme et al., US 2005/0172286 (hereafter Brumme).

4. As per claim 1, Brumme discloses generating a processor instruction proxy stub associated with one or more processor instructions (Par. 2, In 10-12, proxy / stub relationship & see Par. 42, In 8-12, proxy stub associated with instructions); receiving a managed application program interface associated with a managed runtime environment, the managed application program interface and the managed runtime environment not supporting the one or more processor instructions (Par. 25, In 1-12, managed API associated with a managed runtime environment where managed runtime does not support processor instruction & see Fig. 1-2); replacing a portion of the

managed application program interface with native code supporting the one or more processor instructions to generate an optimized managed application program interface; and compiling the optimized managed application program interface including the native code using a compiler of a managed runtime environment (Par. 1, In 1-8, a managed computing environment compiles managed code into native code for certain code that is deemed inappropriate for the particular managed code environment, Par. 4, In 7-8, resulting in significant performance increases and optimization).

5. As per claim 2, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub at a layer associated with a virtual machine of a managed runtime environment (Brumme, Par. 2, In 1-18, CLR is a Microsoft virtual machine of a managed runtime environment & Par. 42, proxy stub associated with layer of virtual machine).

6. As per claim 3, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub during installation of a managed runtime application (Par. 42, In 18-22, proxy stub associated with instructions generated during installation of managed runtime software).

7. As per claim 5, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub via marshaling language code of a virtual machine (Par. 42-45, proxy / stub marshaling of virtual machine).

8. As per claim 6, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one ore more processor instructions of the processor comprises generating the processor instruction proxy stub in response to identifying the processor associated with the one or more processor instructions (see Par. 14 & Fig. 4, resource identification precedes generating proxy stub).

9. As per claim 7, the teachings of Brumme substantially disclose the invention as claimed and further disclose enabling a feature associated with the one or more processor instructions during execution of a managed runtime application based on the optimized managed application program interface (see Par. 30, enabling extended files or types to be compiled during execution based on the optimization process).

10. As per claim 8, it is a system claim with the same limitations as the method in claim 1 and is rejected under the same reasons as claim 1 above.

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11. As per claim 9, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub at a layer associated with a virtual machine of a managed runtime environment (Brumme, Par. 2, In 1-18, CLR is a Microsoft virtual machine of a managed runtime environment & Par. 42, proxy stub associated with layer of virtual machine).

12. As per claim 10, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub during installation of a managed runtime application (Par. 42, In 18-22, proxy stub associated with instructions generated during installation of managed runtime software).

13. As per claim 12, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub via marshaling language code of a virtual machine (Par. 42-45, proxy / stub marshaling of virtual machine).

14. As per claim 13, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated

with the one or more processor instructions of the processor comprises generating the processor instruction proxy stub in response to identifying the processor associated with the one or more processor instructions (see Par. 14 & Fig. 4, resource identification precedes generating proxy stub).

15. As per claim 14, the teachings of Brumme substantially disclose the invention as claimed and further disclose enabling a feature associated with the one or more processor instructions during execution of a managed runtime application based on the optimized managed application program interface (see Par. 30, enabling extended files or types to be compiled during execution based on the optimization process).

16. As per claim 15, the teachings of Brumme substantially disclose the invention as claimed and further disclose the machine accessible medium comprises one of a programmable gate array, application specific integrated circuit, erasable programmable read only memory, read only memory, random access memory, magnetic media, and optical media (Par. 51, ln 10-15, random access memory).

17. As per claim 16, it is an apparatus claim with the same limitations as the method in claim 1 and is rejected under the same reasons as claim 1 above.

18. As per claim 17, the teachings of Brumme substantially disclose the invention as claimed and further disclose the processor instruction proxy stub generator is integrated into one of a virtual machine and the compiler (Par. 29, virtual machine... compiler).

19. As per claim 18, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions of the processor comprises generating the processor instruction proxy stub in response to identifying the processor associated with the one or more processor instructions (see Par. 14 & Fig. 4, resource identification precedes generating proxy stub).

20. As per claim 21, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub at a layer associated with a virtual machine of a managed runtime environment (Brumme, Par. 2, ln 1-18, CLR is a Microsoft virtual machine of a managed runtime environment & Par. 42, proxy stub associated with layer of virtual machine).

21. As per claim 22, the teachings of Brumme substantially disclose the invention as claimed and further disclose enabling a feature associated with the one or more processor instructions during execution of a managed runtime application based on the



optimized managed application program interface (see Par. 30, enabling extended files or types to be compiled during execution based on the optimization process).

***Claim Rejections - 35 USC § 103***

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. Claims 4, 11, 19 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brumme.

24. As per claim 4, the teachings of Brumme substantially disclose the invention as claimed but do not explicitly disclose a Streaming SIMD Extension instruction, an SSE2 instruction, and a MultiMedia Extension instruction. Moreover, SSE, SSE2 and MMX are commonly known in the art as common forms of processor instruction sets.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Brumme to include SSE, SSE2 and MMX in order to optimize an API performance for different kinds of processors utilizing various instruction sets and thereby reaching a larger audience of users.

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25. As per claim 11, the teachings of Brumme substantially disclose the invention as claimed but do not explicitly disclose a Streaming SIMD Extension instruction, an SSE2 instruction, and a MultiMedia Extension instruction. Moreover, SSE, SSE2 and MMX are commonly known in the art as common forms of processor instruction sets.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Brumme to include SSE, SSE2 and MMX in order to optimize an API performance for different kinds of processors utilizing various instruction sets and thereby reaching a larger audience of users.

26. As per claim 19, the teachings of Brumme substantially disclose the invention as claimed but do not explicitly disclose a Streaming SIMD Extension instruction, an SSE2 instruction, and a MultiMedia Extension instruction. Moreover, SSE, SSE2 and MMX are commonly known in the art as common forms of processor instruction sets.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Brumme to include SSE, SSE2 and MMX in order to optimize an API performance for different kinds of processors utilizing various instruction sets and thereby reaching a larger audience of users.

27. As per claim 23, the teachings of Brumme substantially disclose the invention as claimed but do not explicitly disclose a dynamic random memory (DRAM) to store one or more optimized managed application program interfaces or a processor coupled to the DRAM. Moreover, DRAM is commonly known in the art as a type of volatile

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memory with structural simplicity that enables it to achieve very high densities and is a common design choice in systems that utilize random access memory. One of ordinary skill in the art, at the time the invention was made, would have modified the RAM as taught by Brumme to include DRAM in order to achieve higher densities of memory.

28. As per claim 24, the teachings of Brumme substantially disclose the invention as claimed but do not explicitly disclose a Streaming SIMD Extension instruction, an SSE2 instruction, and a MultiMedia Extension instruction. Moreover, SSE, SSE2 and MMX are commonly known in the art as common forms of processor instruction sets.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Brumme to include SSE, SSE2 and MMX in order to optimize an API performance for different kinds of processors utilizing various instruction sets and thereby reaching a larger audience of users.

29. As per claim 25, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub at a layer associated with a virtual machine of a managed runtime environment (Brumme, Par. 2, ln 1-18, CLR is a Microsoft virtual machine of a managed runtime environment & Par. 42, proxy stub associated with layer of virtual machine).

30. As per claim 26, the teachings of Brumme substantially disclose the invention as claimed and further disclose generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub during installation of a managed runtime application (Par. 42, In 18-22, proxy stub associated with instructions generated during installation of managed runtime software).

31. As per claim 27, the teachings of Brumme substantially disclose the invention as claimed and further disclose enabling a feature associated with the one or more processor instructions during execution of a managed runtime application based on the optimized managed application program interface (see Par. 30, enabling extended files or types to be compiled during execution based on the optimization process).

### ***Response to Arguments***

32. Applicant's arguments, see REMARKS, filed 11/30/2007, with respect to the rejection(s) of claim(s) 1-27 under D'Inverno (EP 1 313 012) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Brumme et al., US 2005/0172286.

***Conclusion***

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL R. FATEHI whose telephone number is (571)270-1407. The examiner can normally be reached on M-F 10:30AM-7PM EST.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Parham (Paul) R Fatehi/  
Examiner, Art Unit 2194

/Meng-Ai An/

Supervisory Patent Examiner, Art Unit 2195